REMARKS

The Examiner has rejected claims 1-3 under 35 U.S.C. 103(a) as unpatentable over Otterness et al, U.S. Patent 6,460,122 and Akashi et al, U.S. Patent 6,438,658. The examiner rejected claims 4-6, 8 and 10 as unpatentable over Otterness et al, U.S. Patent 6,460,122 and Akashi et al, U.S. Patent 6,438,658 and further in view of Dean et al, U.S. Patent 6,604,174. The examiner rejected claim 9 over Otterness et al, U.S. Patent 6,460,122, Akashi et al, U.S. Patent 6,438,658 and Dean et al, U.S. Patent 6,604,174, further in view of Itskin, U.S. Patent 5,809,537. The examiner rejected claim 11 as unpatentable over Otterness et al, U.S. Patent 6,460,122, Akashi et al, U.S. Patent 6,438,658 and Dean et al, U.S. Patent 6,604,174, further in view of Noel et al, U.S. Patent 6,381,682.

Applicant has found that U.S. Patent 6,438,658 is to Baliga. Applicant believes that the Examiner meant U.S. Patent 6,438,653 to Akashi because some text quoted by the examiner in the action matches text in '653, and because Akashi is listed as 6,438,653 on the form 892 attached to the action.

In the Specification

The Examiner has requested amendment of several informalities in the specification and abstract. Paragraphs 1, 27, and 33 have been amended in the Specification as requested. Paragraphs 19 and 30 have also been amended to correct minor typographical errors; no new matter has been introduced. The abstract has also been shortened to ensure it contains fewer than 150 words.

In the Claims

Independent claims 1 and 5 have been amended to more clearly indicate the role of the dynamically allocable cache blocks in the invention as claimed, and to more clearly distinguish the invention as claimed from that of Otterness, '122. Otterness discloses a caching disk controller with RAID (redundant array of independent drives) functions, while the present invention describes a memory cache.

Otterness Describes Non-Analogous Art

U.S. Patent 6,460,122 to Otterness, et. al., discloses an input/output controller capable of storing data in redundant form on a disk memory system. The input/output

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controller system of Otterness includes disk caching functions, where a section of RAM memory holds a copy of data present on the disk.

The present application describes a memory cache for caching main memory contents for access by a processor.

While both Otterness's caching disk controller, and the present application's memory cache use a smaller, relatively fast, memories to avoid referencing large, slow, memories when recently-used information is reused; they are very different portions of a computer system with greatly different performance and design requirements. The differences are so extensive that the hardware of a memory cache bears very little resemblance to that of a caching disk controller.

For example, a caching disk controller typically is implemented with an embedded processor 102 of Otterness Fig 2. The cache memory (110 Otterness) is implemented as a RAM, with cache control implemented by firmware in a ROM or RAM (104 Otterness) executing on the embedded processor (102 Otterness). Variations on this basic architecture exist, some functions such as compression and error detection may be hardware-assisted, and the embedded processor (102 Otterness) of a caching disk controller may include a memory cache.

A memory cache typically has no embedded processor, with cache control and cache hit recognition performed by specialized hardware. A memory cache typically must respond to cache hits in one or a few clock cycles. A memory cache is of no use unless it is faster to access than the few tens of nanoseconds required to access a large RAM memory. A caching disk controller has more time to respond since uncached disk accesses may require many milliseconds for mechanical rotational delay and head-seek operations.

The disk cache system of Otterness contains memory cache, such as XOR processor memory cache 110. Otterness describes, Col 4 line 32 through Col 5 line 28, issues regarding cache coherency of this memory cache. The internal memory cache of Otterness lacks the dynamic allocation of memory blocks to individual caches of the present application

Memory cache designers ordinarily do not consult caching disk controller art because the need for far shorter response time in a memory cache prohibits use of typical disk controller architectures and eliminates many disk controller features as

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impractical. Memory cache designers are more likely to consult references specifically relevant to memory cache. Memory cache designers are therefore unlikely to include Otterness's teachings in memory cache designs, or to think of combining Otterness's teachings with those of Akashi.

Claims 1 – 3

Claim 1 has been amended to clarify that the claim applies to a memory cache, not to a disk cache such as described by Otterness. Since Claims 2-3 depend on Claim 1, this amendment limits the scope of those claims also, such that they also should not be obvious under 35 U.S.C. 103 over Otterness and Akashi because a designer having Akashi would typically not refer to Otterness while designing a memory cache.

Claims 4-5, 8, 10, and 11

Claim 1 (parent claim of Claim 4), and claim 5 (parent claim of Claims 8, 10, and 11) have been amended to clarify that the claim applies to a memory cache, not to a disk cache such as described by Otterness. These claims should not be obvious under 35 U.S.C. 103 over Otterness, Akashi, and Dean because a designer having Akashi and Dean would typically not refer to Otterness while designing a memory cache.

Claims 7, 9

Parent claim 5 has been amended to clarify that these claims applies to a memory cache, not to a disk cache such as described by Otterness. Claims 7 and 9 should not be obvious under 35 U.S.C. 103 over Otterness, Akashi, Dean, and Itskin because a designer having Akashi, Dean and Itskin (describing memory cache art), would typically not refer to disk cache art such as Otterness while designing a memory cache.

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CONCLUSION

Applicant therefore respectfully requests that the examiner enter the foregoing amendment and submits that all grounds for rejection have been overcome.

Respectfully submitted,

By: _____

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